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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,558	HILL ET AL.	
	Examiner	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED FINAL ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12 rejected under 35 U.S.C. 102(b) as being anticipated by No. 5,898,893 to Alfke.

3. In reference to Claim 1, Alfke discloses a method for asynchronously transferring data, said method comprising:

Providing a buffer device (Fig. 1, elements 100 and 101);

Defining in the buffer device a plurality of buffer segments (Fig. 1, element 101, indicated by the 4 bits write and read addresses, $W_3 - W_0$ and $R_3 - R_0$;

Filling buffers segments with data from at least one data source device (indicated by DIN signal bus in Figure 1) operating in a respective clock domain (indicated by the write clock signal line, W-CLK); and

Upon any respective buffer segment being filled up (e.g., written to) with said data, generating an indication of availability of the data contents of said respective buffer segment for transfer to at least one data destination device (in Alfke's method, the read enable signal, RE in Fig. 1, is an indication to the destination device of the availability of the contents at a particular read address) operating in a respective clock domain (indicated by the read clock signal line, R-CLK), being asynchronous to the source device (Column 3, lines 3-5).

4. In reference to Claim 2, Alfke discloses the method of Claim 1 wherein upon the contents of the respective buffer segment being acknowledged as transferred to the data destination device (the read address will increment to the next buffer segment address and the read counter 103 will increment by 1), generating an indication of availability of that buffer segment for further refilling with data from the source device (the WE, Write Enable, signal line from Fig. 102 will be asserted when the write address points to the buffer segment).

5. In reference to Claim 3, Alfke discloses the method of Claim 2 wherein the generating of the respective indications of buffer segment availability comprises determining the state of a respective buffer gauge signal uniquely associated with each buffer segment. The gauge signal here is the write counter, read counter, full and empty logic (Fig. 1, elements 102, 103, 105, and 106 respectively) associated with each buffer segment. It determines whether the segment can be written to, WE signal line, or read from, RE signal line.

6. In reference to Claim 4, Alfke discloses the method of Claim 3 wherein the buffer gauge signal uniquely associated with each buffer segment comprises a single-bit signal, which is the full logic or empty logic single-bit flag indicated in Fig. 1, elements 105 and 106.

7. In reference to Claim 5, Alfke discloses the method of Claim 4, wherein in the event the state of the respective buffer gauge signal indicates the buffer segment is full, the indication of availability of the buffer segment contents to the data destination is triggered. This is implemented by the RE signal being active when the full flag, Fig. 1, element 106, is asserted.

8. In reference to Claim 6, Alfke discloses the method of Claim 4 wherein in the event the state of the respective buffer gauge signal indicates the buffer segment is empty, the indication of availability of that buffer segment for further refilling of data from the source device is triggered.

This is implemented by the WE signal being active when the empty flag, Fig. 1, element 105, is asserted.

9. In reference to Claims 7 and 11, Alfke discloses the method and device of Claims 1 and 8, respectively, wherein defining of the plurality of buffer segments comprises adjusting the number and/or size of the buffer segments within a selectable range. This is inherent in Alfke's design, since he uses the Xilinx XC4000 FPGA (Column 4, lines 35-42). See attached Application Note on using select-RAM Memory in XC 4000 Series FPGA and Fig. 1 in application note.

10. In reference to Claim 8, Alfke discloses a data transfer controller (Fig. 1) for asynchronously transferring data (Fig. 1, R-CLK and W-CLK clock signals) by way of a buffer device (Fig. 1, elements 101), the controller comprising:

A buffer-segment module (Fig. 1, elements 102 and 103) configured to define a plurality of buffer segments in the buffer device (Fig. 1, $W_3 - W_0$ and $R_3 - R_0$ addresses, in other words, 16 different buffer segments), said buffer segments filled with data from a least one data source device (Fig. 1, DIN signal bus) operating in a respective clock domain (Fig. 1, W-CLK signal line); and

A segment availability gauge (Fig. 1, elements 102, 103, 105 and 106) configured to generate, upon any respective buffer segment being filled up with said data, an indication of the availability of the data contents of the respective buffer segment for transfer to at least one data destination device operating in a respective clock domain (Fig. 1, RE signal is asserted when there is something written to a buffer segment and it is available for transferring through DOUT bus line to destination device; R-CLK is the read clock of the destination device). The segment-

availability gauge being further configured to generate, upon the contents of the respective segment being acknowledged as transferred to the destination device, an indication of availability of that buffer segment for further refilling data from the source device (Fig. 1, WE signal is asserted when one can write to the buffer segment from the source device through DIN bus line). The write clock (Fig. 1, W-CLK signal) can be asynchronous to the read clock (Fig. 1, R-CLK and Column 3, lines 3-5).

11. In reference to Claim 9, Alfke discloses the controller of Claim 8 wherein a segment-availability gauge comprising a comparator (Fig. 1, element 106) configured to determine whether the state of a respective single-bit signal (Fig. 1, indicated by the FULL signal) uniquely associated with a respective buffer segment is indicative of whether the respective buffer segment is full.

12. In reference to Claim 10, Alfke discloses the controller of Claim 9 wherein the comparator (Fig. 1, element 105) is further configured to determine whether the state of the single-bit (Fig. 1, indicated by the EMPTY signal) associated with that buffer segment is indicative of whether the respective buffer segment is empty.

13. In reference to Claim 12, Alfke discloses a system for asynchronously transferring data (Fig .1), the system comprising:

A data buffer device (Fig. 1, element 101);

A buffer-segment module (Fig. 1, elements 102 and 103) configured to define a plurality of buffer segments in the buffer device (Fig. 1, element 101), respective ones of the buffer segments being filled with data from at least one data source device operating in a respective clock domain (Fig. 1, W-CLK); and

A segment availability gauge (Fig. 1, elements 102, 103, 105 and 106) configured to generate, upon any respective buffer segment being filled up with said data, an indication of the availability of the data contents of the respective buffer segment for transfer to at least one data destination device operating in a respective clock domain (Fig. 1, RE signal is asserted when there is something written to a buffer segment and it is available for transferring through DOUT bus line to destination device; R-CLK is the read clock of the destination device), the indication based on a single-bit signal uniquely associated with the respective buffer segment to indicate whether the buffer segment is full (Fig. 1, indicated by the FULL signal). The segment-availability gauge being further configured to generate, upon the contents of the respective buffer segment being acknowledged as transferred to the destination device, an indication of availability of that buffer segment for further refilling of data from the source device (Fig. 1, WE signal is asserted when one can write to the buffer segment from the source device through DIN bus line), the indication based on whether the single-bit signal indicates the buffer segment is being empty (Fig. 1, indicated by the EMPTY signal). The write clock (Fig. 1, W-CLK signal) can be asynchronous to the read clock (Fig. 1, R-CLK and Column 3, lines 3-5).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 13 is rejected under 35 USC 103(a) as being unpatentable over Alfke.

Alfke discloses the system of Claim 12, where the segment-availability gauge (Fig. 1, elements 102, 103, 105 and 106) includes a counter comprising D flip-flops (Fig. 3a, elements 201, 203, 204, and 207) configured to count data words transferred to the buffer module. The segment-availability gauge further include a logic module (Fig. 1, elements 106) coupled to the counter to set the respective signal indicative of the buffer segment being full (Fig. 1, element 106 and the FULL signal line) when the counter reaches the maximum data word count. Alfke does not expressly disclose the counter being coupled to a register to count data words transferred to the buffer.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use D flip-flops as the memory storage element for counting means in order to implement the function of the register.

The suggestion/motivation for doing so would have been to use standard memory logic to implement a register, which is a general term for storage of various types of data words.

Therefore, it would have been obvious to use D flip-flops to implement the register to count data words, to obtain the invention as specified in Claim 13.

16. Claim 14 is rejected under 35 USC 103(a) as being unpatentable over Alfke.

Alfke discloses the system of Claim 13, where the logic module (Fig. 1, element 106) is attached to a counter (Fig. 1, element 106) that is responsive to an enable signal line (Fig. 1, WE) associated with the destination device that determines when the source device can write data to the buffer device (Fig. 1, element 101). Alfke does not expressly disclose an acknowledge signal from the data destination device that indicates the buffer can be written to or refilled.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Alfke's system such that the acknowledge signal is the WE signal whose status can be determined by the destination device after it has read from the buffer.

The suggestion/motivation for doing so would have been a simple and logical way to implement the WE signal of Alfke's device. If the destination device has read from the buffer, it is clear data can now to written to the now empty memory segment where data was read from, hence the WE signal line can be asserted.

Therefore, it would have been obvious to set the WE signal as the acknowledge signal linked to the data destination device to obtain the invention as specified in Claim 14.

Response to Arguments

17. Applicant's arguments filed 01/26/2004 have been fully considered but they are not persuasive.

18. The main issue of contention is the definition of a buffer segment. Strictly from the claim language, the buffer segment can be elements of any buffer, e.g., one element consisting of a plurality of bits, the entire element written to or read from on one clock cycle. For instance, Fig. 1 of applicant's shows the buffer segments in a stack, each segment can be a single word that is written per clock cycle. Similarly, this is the case with Alfke, where in Fig. 1, element 101, each element of the dual-port memory is written to/read from on one clock cycle, e.g., on increment of the write or read counters. Claim 1 does not place any limitations on the size/depth of the buffer segments. Therefore anticipation is proper.

19. Applicant notes "Claim 1 is directed to a method for asynchronously transferring data by way of a buffer device. A_plurality of buffer segments is defined in the buffer device. A filling action allows to fill respective ones of the buffer segments with
data from a data source device. Upon any respective buffer segment being filled up with such data, a generating action allows to generate an indication of availability of the data contents of the respective buffer segment for transfer to a data destination device". Alfke discloses this as shown in Fig. 1. Two clocks exist, one for reading and another for writing, hence providing asynchronous transfer of data. The plurality of buffer segments is indicated by the counter size. Data is clearly transferred from DIN, the source of the data. Whenever any element/segment of the dual-port memory is written to, the write counter is incremented, and hence, as long as the full logic is not asserted, the data contents are available for read (the indicator in this case is can be thought of as the signal level of the full flag, element 106). Furthermore, the claims do not preclude a fullness indication by Alfke's counters.

20. Applicant argues that Alfke does not define any buffer segments in his FIFO and that the segments are in the counters and not the buffer device. Examiner points out that the segments must be defined already in the dual-port memory, otherwise, each write/read will not know where to put/pull the information from. The address of where to write is already predetermined. As with almost all FIFO, there is base address where the write/read occurs. Each segment is defined based on the offset from the size of the data word. Furthermore, claim 1 only sets forth "defining" without specifying what the definition is.

21. Applicant argues that Alfke does not teach or suggest the concept of buffer segments that are either filled (or drained) with actual data to be transferred. Examiner wishes to point out that

each time a write of actual data to the FIFO occurs in Alfke, a buffer segment is being filled and similarly, each time a read of actual data from the FIFO occurs in Alfke, a buffer segment is being emptied.

22. Applicants arguments to claims 8 and 12 are similarly rebutted with Examiner's arguments from above.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
2/27/2004

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